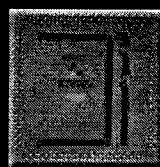


HTMT

REALIZATION OF SUPERCONDUCTOR VLSI



Shift Registers

FIRST FAB RUN April 2000

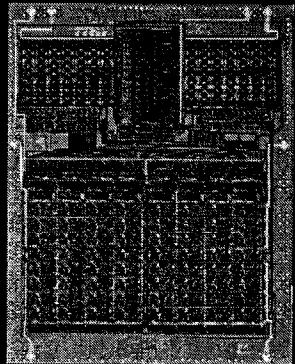
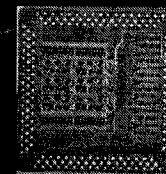
Initial 4 kA/cm² process run

- Shift register (SR) tests (4, 16, 64, and 256 bits long (12 J/s/bit))
- Individual gate (logic, memory, I/O) and transmission line tests
- Thermal noise, electrical pulse jitter test

THIRD FAB Dec. 2000

All components for FLUX

- | | |
|--------------------|---------------------------------|
| · Individual gates | · First stage decoder |
| · Clock controller | · New memory cells |
| · Registers | · Transmission lines expts. |
| · ALU slice | · Interface parts / scan path |
| · Program counter | · Off-chip communications tests |

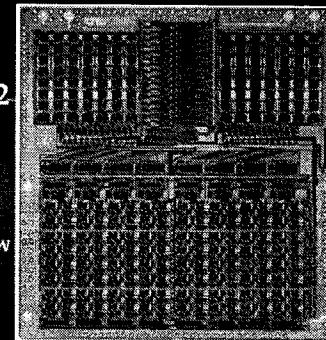


FLUX-1 Sept. 2001

- 10.65 mm x 13.2 mm chip
- 1.75 μ m, 4 kA/cm² Nb technology
- 20 GHz internal clock (design)
- 5 GByte/sec inter-chip data transfer
- Scan path diagnostics included
- 65000 junctions, 5000 gate equivalent
- Power dissipation ~ 5 mW @ 4.5K
- 40 GOPS peak computational capability (8 bits @ 20-GHz clock)
- Engineering flaws discovered during test

FLUX 1R1 Aug. 2002

- 10.65 mm x 10.65 mm
- 63000 junctions
- 25 GHz clock (design)
- Power dissipation ~ 9.2 mW
- Currently under test



TRW

**STONY
BROOK**
STATE UNIVERSITY OF NEW YORK